

Module-4

7	a.	Explain any four roles or importance of Small Scale Industries (SSI) in e	economic				
		development. (0	08 Marks)				
	b.	Define Ancillary Industry and Tiny Industry.					
	c.	Outline any four reasons for sickness in SSI sector. (0	04 Marks)				

OR

8 Summarize any four state level or central level institutions that support small business (16 Marks) enterprises.

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

15ES/EI51

Module-5

List out any four characteristics of project. 9 a.

(04 Marks) Classify projects into different types based on various parameters. (05 Marks)

- b. What is project formulation? Explain the major steps involved in project formulation. с.
 - (07 Marks)

OR

- Mention various steps involved in the PERT analysis. (10 Marks) 10 a.
 - List out the advantages and limitations of CPM. b.
 - Show the relation between project design and network using block diagram. с.

(04 Marks)

(02 Marks)

		CBCS SCHEME	
USN			15EC52
		Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019	
		Digital Signal Processing	
Tin	ne:	3 hrs. Max. Mar	ks: 80
	No	ote: Answer any FIVE full questions, choosing ONE full question from each mod	ule.
		Module-1	
1	a.	Derive the DFT expression from the DTFT. (0	04 Marks
	b.		06 Marks
	c.	Find the circular convolution between the sequences using DFT and IDFT method	06 Marks
		$x_1(n) = (1, 2, 3, 1) \text{ and } x_2(n) = (4, 3, 2, 1)$ (0)	06 Marks
		OR	
2	a.	State and prove that circular (i) Folding ii) Frequency shift properties of an S	N' poir
	1.	sequence. (0	06 Marks
	D.	Consider the finite length sequence $x(n) = \delta(n) + 2\delta(n-j)$ Find : (i) 10 point DFT of $x(n)$	
		(ii) $y(k) = e^{-j\left(\frac{4\pi k}{10}\right)}X(k)$ where X(k) is 10 point DFT of x(n) find y(n)	
		(ii) $y(k) = e^{-(10)}X(k)$ where X(k) is 10 point DFT of x(n) find y(n) (iii) Find z(n) that has DET z(k) = X(k) and a more (k) is (1 - 10).	
		(iii) Find z(n) that has DFT z(k) = X(k).w(k) where w(k) is the 10 point DFT of w(n) = u(n) - u(n - 7) (0)	07 Marks
	c.	Let $x(n)$ be a finite length sequence with $x(k) = \{1, 4j, 0, -4j\}$, find the DFT's of	IT THEFT
		(i) $x_1(n) = e^{j\frac{\pi}{2}n} x(n)$ (ii) $x_2(n) = \cos\left(\frac{\pi}{2}n\right) x(n)$ (iii) $x_3(n) = x((n-1)_4)$ (0)	03 Marks
		Module-2	
3	a. b.		04 Marks
		$x(n) = \{2, 1, -1, 2, -3, 5, 6, -1, 2, 0, 2, 1\}$. Using overlap and save method. Use	e 8 poir
	c.	circular convolution in your approach. (1	10 Marks
	с.	State and prove symmetric property of twiddle factor w_N . (0)	02 Marks
		OR	
4	a.	Find the number of complex multiplications and additions required to computer 1 DFT using (i) Direct method (ii) FFT (iii) what is the speed improvement (iv) Number of real registers needed (v) Number of trigonometric functions needed	nt facto I.
	b.		(n) usin
		Module-3	
5	a.)8 Marks

a. Develop 8 point DIT-FFT radix - 2 algorithm and draw the signal flow graph. (08 Marks)
b. Find the 8 point DFT of the sequence x(n) = {1, 1, 1, 1, 0, 0, 0, 0} using radix - 2 DIF FFT algorithm. (08 Marks)

OR

- Find the 4 point circular convolution of x(n) and h(n) given below using radix 2 DIT FFT 6 a. (06 Marks) algorithm. $x(n) = \{1, 1, 1, 1\} h(n) = \{1, 0, 1, 0\}.$
 - b. First five points of 8-point DFT's of a real valued sequence is given by x(0) = 0x(1) = 2 + 2j, x(2) = -4j, x(3) = 2 - 2j, x(4) = 0. Determine the remaining points. Hence find the sequence x(n) using radix – 2 DIT FFT algorithm. (10 Marks)

Module-4

- (04 Marks)
- b. Design an analog lowpass Butterworth filter for the following specifications $0.8 \leq \left|H_{a}\left(s\right)\right| \leq 1, 0 \leq \Omega \leq 0.2\pi, \ \left|H_{a}\left(s\right)\right| \leq 0.2, 0.6\pi \leq \Omega \leq \pi \,.$ (08 Marks) (04 Marks)
- Explain Analog to Analog transformation. C

Compare Butterworth and Chebyshev filters.

OR

- Design a digital lowpass filter using BLT to satisfy the following chart. 8 a.
 - i) Monotonic pass and stop band
 - ii) $-3 dB cut off of 0.5\pi rad$
 - (08 Marks) iii) Magnitude down at least 15dB at 0.75π rad
 - using Impulse Invariant Transformation b. Find H(z) for the given T.F H(s)(08 Marks)

(IIT) technique.

7

a.

Module-5

- Obtain direct form I, Form II, Cascade and parallel form of realization for the following 9 a. system. y(n) = 0.75 y(n-1) - 0.125 y(n-2) + 6x(n) + 7x (n-1) + x(n-2). (12 Marks)
 - $\left(\frac{1}{2}\right)^{n}$ [u(n) u(n 4)] using direct form I. (04 Marks) Realize an FIR filter given by h(n) =b.

OR

Write equations of any four different windows used in design of FIR filters. (10 Marks) 10 a. b. Design the symmetric FIR, lowpass filter whose desired frequency response is given as

 $H_{d}(w) = \begin{cases} e^{-jw\tau} \text{ for } |w| \le w_{c} \\ 0 \text{ otherwise} \end{cases}$

The length of the filter should be 7 and $w_c = 1$ radian/sample use rectangular window.

(06 Marks)

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		CBCS SCHEME
USN		15EC53
		Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2019 Verilog HDL
Tin	ne:	3 hrs. Max. Marks: 80
	Λ	ote: Answer any FIVE full questions, choosing ONE full question from each module.
1	a. b.	Module-1 (06 Marks) Explain top-down design methodology with an example. (06 Marks) Explain the typical design flow for designing VLSI IC circuits, with a neat flow chart. (10 Marks)
2	a. b.	OR(06 Marks)Explain Bottom-up design methodology with an example.(06 Marks)Explain the different levels of abstraction used for programming in verilog.(10 Marks)
3	а. b. c.	Module-2 Explain system tasks and compiler directives in verilog. (06 Marks) What are the basic components of a module? Explain all the components of a verilog module with a neat block diagram. (06 Marks) Write verilog description of SR Latch. Also write stimulus code. (04 Marks)
4	a. b.	OR Write a note on: i) Registers ii) Nets iii) Arrays iv) Parameters v) Vectors vi) Memories. (12 Marks) Declare a top-level module "Stimulus". Define Reg_in (4 bit) and Clk (1 bit) as register variables and Reg_out (4 bits) as wire. Instantiate the module "shift-reg" in "stimulus" block and connect the ports by ordered list. Declare A (4 bit) and clock (1 bit) as inputs and B (4 bit) as output in "shift-reg" module. (No need to show internals). Write a verilog code for the above. (04 Marks)
5	а. b .	Module-3Write the verilog description of 4 bit ripple carry adder at gate level abstraction, with a neat block diagram. Also, write stimulus block.(08 Marks)What would be the output of the following: $a = 4'b1010$, $b = 4'b1111$ i) a & biii) & a iii) & a
		$V(1) a \land b = V(11) z = \{a, b\}.$ (08 Marks)

OR

6 a. A full subtractor has three 1-bit inputs x, y and z (previous borrow) and two 1-bit outputs D(Difference) and B(Borrow). The logic equations are

 $D = \overline{x yz} + \overline{x yz} + \overline{x yz} + x yz$

 $\mathbf{B} = \mathbf{x}\mathbf{y} + \mathbf{x}\mathbf{z} + \mathbf{y}\mathbf{z}$

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 – 50, will be treated as malpractice.

Write verilog description using dataflow modeling. Instantiate the subtractor module inside a stimulus \mathbb{E} lock and test all possible combinations of inputs x, y and z. (08 Marks)

(04 Marks)

b. Design 4:1 multiplexer using gate level modeling or structural description. Write stimulus block. (08 Marks)

Module-4

7	a.	Explain structured procedure statements in werilog.	(06 Marks)
	b.	Write a verilog behavioral 8:1 multiplexer program using case statement.	(06 Marks)
	с.		(04 Marks)
		OR	
8	a.	Explain procedural assignment statements in verilog.	(06 Marks)
	b.	Explain sequential and parallel blocks with examples.	(06 Marks)
	с.	Write a verilog code to find the first bit with a value 1 in	

Write a verilog code to find the first bit with a value 1 in $Flag = 16'b \ 0010 \ 0000 \ (0000 \ 0000)$.

Module-5

9	a.	Explain the design tool flow followed in VLSI design with a neat flow diagram.	(10 Marks)
	b.	Write VHDL Data flow description of 1 Bit full Adder.	(06 Marks)

OR

- 10 a. Explain the relationship between a design entity and its entity declaration and architecture body in VHDL. (10 Marks)
 - b. Write VHDL structural description of 1 Bit Full Adder. (06 Marks)



c. An information source produces a sequence of independent symbols having the following probabilities. Construct binary code using Huffman encoding and find its efficiency. (06 Marks)



OR

- State Kraft McMillan Inequality property. 4 a.
 - Consider a discrete memory less source with S = (X, Y, Z) with the corresponding b. probabilities P = (0.5, 0.3, 0.2). Find the code words for the symbols using Shannon's algorithm. Also, find the source efficiency and redundancy. (06 Marks)
 - c. Consider a discrete memory less source with S = (X, Y, Z) with respective probabilities P = (0.6, 0.2, 0.2). Find the codeword for the message 'YXZXY' using arithmetic coding.

(06 Marks)

(04 Marks)

Module-3

A binary channel has the following characteristics 5 a.

 $\begin{vmatrix} 2 \\ 3 \\ 1 \\ 3 \end{vmatrix} \begin{vmatrix} 3 \\ 3 \\ 3 \end{vmatrix}$

. If input symbols are transmitted with probabilities $\frac{3}{4}$ and $\frac{1}{4}$

(03 Marks) respectively. Find entropies, H(X), H(X, Y) and H(Y/X).

- b. Prove that the mutual information is always a non negative entity $I(X; Y) \ge 0$. (06 Marks)
- The noise characteristics of a channel are as shown in fig.Q5(c). Find the capacity of the C. (07 Marks) channel using Muroga's method.



(04 Marks) State the properties of Joint Probability Matrix. 6 a. b. Find the mutual information for the channel shown in fig.6(b). Let $P(x_1) = 0.6$ and (06 Marks) $P(x_2) = 0.4.$



Derive the expression for the channel capacity of a Binary Symmetric Channel. (06 Marks) C.

Module-4

- 7 a. For a (6, 3) code find all the code vectors if the co-efficient matrix P is given by
 - $\mathbf{P} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$

i) Find code vector ii) Implement the encoder iii) Find the syndrome vector (S). iv) Implement the syndrome circuit. (08 Marks)

b. Obtain the generator and parity check matrices for an (n, k) cyclic code with $g(x) = 1+x+x^3$.

(08 Marks)

OR

- 8 a. In an LBC, the syndrome is given by
 - $S_1 = r_1 + r_2 + r_3 + r_5$; $S_2 = r_1 + r_2 + r_4 + r_6$; $S_3 = r_1 + r_3 + r_4 + r_7$.
 - i) Find the parity check matrix (H) ii) Draw the encoder circuit
 - iii) Find the code word for all input sequences.
 - iv) What is the syndrome for the received data 1011011? (08 Marks)
 - b. In a (15,5) cyclic code, the generator polynomial is given by $g(x) = 1+x+x^2+x^4+x^5+x^8+x^{10}$. Draw the block diagram of an encoder and syndrome calculator for this code. Find whether $r(x) = 1+x^4+x^6+x^8+x^{14}$ a valid code word. (08 Marks)

Module-5

- 9 a. Design a (15,7) binary BCH code with r = 2. (06 I b. Consider the (3, 1, 2) convolution code with $g^{(1)} = (1 \ 1 \ 0), g^{(2)} = (1 \ 0 \ 1), g^{(3)} = (1 \ 1 \ 1).$
 - b. Consider the (3, 1, 2) convolution code with g² = (1, 1, 0), g² = (1, 0, 1), g² = (1, 1, 1).
 i) Find the constraint length ii) Find the rate iii) Draw the encoder block diagram iv) Find the generator matrix v) Find the code word for the message sequence (1, 1, 1, 0, 1) using time domain and transfer domain approach. (10 Marks)

OR

- 10 a. Explain why (23, 12) Golay code is called as perfect code.
 - b. Consider the convolution encoder shown in fig. Q10(b).
 - i) Write the impulse response of the encoder.
 - ii) Find the output for the message (1 0 0 1 1) using time domain approach.
 - iii) Find the output for the message (1 0 0 1 1) using transfer domain approach. (12 Marks)



(04 Marks)

(06 Marks)

		CBCS SCHEME	
USN			15EC553
		Fifth Semester B.E. Degree Examination, Dec.2018/Jan.2	019
		Operating Systems	
Tim	ne: 3	3 hrs. Max	. Marks: 80
		Note: Answer any FIVE full questions, choosing ONE full question from each module.	
		Module-1	
1	a.	Define operating system. Explain the key concerns of an operating system.	(10 Marks
	b.	Explain the different computational structures of operating system.	(06 Marks
		OR	
2	a.	Explain different classes of operating system.	(10 Marks
	b.	Explain various resource allocation strategies.	(06 Marks
		Module-2	
3	a.	Define process, process states and transition with suitable algorithm.	(08 Marks
	b.	Explain Process Control Block.	(08 Marks
		OR	
4	a.	For a given set of process FCFS and SRN scheduling compare their performan	nce in terms o
		mean turnaround time and weighted turnaround time.	(10 Marks
		$\begin{array}{c cccc} Process & P_1 & P_2 & P_3 & P_4 & P_5 \\ \hline \hline \end{array}$	
		Admission time02359Service time33253	
	b.	Explain long-term and short term scheduling.	(06 Marks
	0.	A State of the second sec	(00 marks
5	0	Module-3	(09 M
5	a. b.	Compare contiguous and non-contiguous memory allocation techniques. Write a short note on : i) paging ii) segmentation.	(08 Marks (08 Marks
	0.	de bare	(00 Marks
(Curlain demand and the meliminaria	(10.3.4.1
6	a. b.	Explain demand paging preliminaries. Write short note on :	(10 Marks
	υ.	i) First–In–First–Out (FIFO) page replacement policy.	(03 Marks
		ii) Least Recently Used (LRU) page replacement policy.	(03 Marks
		Module-4	
7	a.	Explain file system and IOCS.	(08 Marks
1	b.	Explain fundamental file organizations.	(08 Marks
		OR	
8	a.	Explain directory structures.	(08 Marks
U	b.	Explain file system action at a file operation.	(08 Marks
9	a.	<u>Module-5</u> Define message passing. Explain how to implement the message passing.	(08 Marks
2	b.	Explain mail boxes and message passing in unix.	(08 Marks
			(
10	0	OR Define deadlock, Explain deadlock in resource allocation.	(08 Marks
10	a. b.	Explain deadlock detection algorithm.	(08 Marks
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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2 Any revealing of identification, anneal to evaluator and /or equations written cg. 42+8 = 50, will be treated as malpractice.

USN	r		15EC56
		Fifth Semester B.E. Degree Examination, Dec.2018 Object Oriented Programming using	
Tin	ne [,] 1	3 hrs.	
1 11		Note: Answer any FIVE full questions, choosing ONE full question from each module.	Max. Marks: 80
		Module-1	
1	а. b. c.	What is C++? List the applications of C++. Describe the structure of a C++ program with an example. When do we use cascading of input/output operators? Give example.	(04 Marks (08 Marks (04 Mark
			(04 Mark
2	a.	OR Write a C++ program to find the sum of digits of a given number. e.g If input number = 16738	
	b.	output is 25 i.e. $1 + 6 + 7 + 3 + 8$. Explain the different types of expressions in C++. Give examples fo	(04 Marks) or each type. (any four (08 Marks)
	C.	With an example, describe the purpose of new and delete operators in	C++. (04 Marks
		Module-2	
3	a. b.	Mention the restrictions posed by the complier on inline functions. Design a class 'triangle' containing data items 'base' 'height' and t setdata(), getdata(), displaydata() and findarea(), to set values to 'ba	ase' and 'height', to ge
	c.	the user input, to display and find area of triangle (i.e. $\frac{1}{2}$ * base*heig the main function which creates the object and uses the members of the Discuss the different types of function overloading in C++.	ght) respectively. Writ ne class. (08 Marks (04 Marks
		OR	
4	a.	When do we use default arguments? State the rules that need to be default arguments.	(04 Marks
	b.	Draw a neat diagram and explain the process of memory allocation to	objects in C++. (06 Marks
	c.	Develop a C++ program to define two classes namely husband and v member 'salary' respectively. Calculate and display the total incom friend function.	wife that hold a privat
~		Module-3	
5	a. b.	How are constructors differ from member functions of a class? What is operator overloading? Give syntax and example. List the op overloaded.	(04 Marks perators that cannot b (06 Marks
	c.	Explain the significance of friend functions to overload operators.	(06 Marks
		OR	
6	a. b.	Discuss the importance of dynamic constructors and destructor in a C+ Write a C++ program to add two complex numbers by overloading overload << and >> operators for reading and displaying the complex	g the + operator. Also
		1 of 2	

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(04 Marks)

(08 Marks)

(04 Marks)

(04 Marks)

Module-4

- What is inheritance? List its advantages. 7 a.
 - Explain the visibility inheritance modes. Give an example. b.
 - Compare multiple inheritances with multilevel inheritance. c.

OR

- What is abstract class? Give an example. 8 a.
 - Demonstrate the working of pointers as objects with a relevant example. (08 Marks) b. (04 Marks)
 - State the differences between virtual and pure virtual functions. c.

Module-5

- What is a data stream? Describe the hierarchy of file stream classes in C++. (08 Marks) 9 a. Explain the following unformatted I/O functions : i) getline() ii) write(). (04 Marks) b.
 - Compare and contrast width() and setw(). C.

OR

- How file opening and closing is done? What are the functions required for reading and 10 a. (08 Marks) writing data in a file. Explain with an example.
 - Create a C++ program to read a text file and find number of characters, words and lines in a b. (08 Marks) file.

- (04 Marks)



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On completing year answers, compulsorily draw diagonal cross lines on the remaining blank pages. ny revealing of identification, append to evaluator and /or equations with Important Note : 1.

(06 Marks)

(06 Marks)

(08 Maris)

(04 Marks)

OR

- a. Explain the role of CALL and subroutines in 8051 microcontroller programming. (04 Marks)
- b. What are timers and counters? Explain its operations.
- c. Explain timer control register and timer mode control register.

Module-5

- 9 a. Explain the 8051 S-CON register.
 - b. Write a 8051 subroutine program to initialize 8051 serial port to operate in mode 0 for transmission. (04 Marks)
 - c. Explain RS 232 standards.

OR

- 10 a. Bring out the difference between interrupts and polling. (04 Marks)
 - b. Explain interrupt priority register of 8051 micracontroller. (04 Marks)
 - c. Write an 8051 C grogram to send letters 'M', 'D' and E to the LCD using delays. (08 Marks)

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